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## In the Claims:

Below is a listing of claims in the Application.

## Listing of Claims:

1. (Currently Amended) A system for arbitrating access to a shared resource comprising:

a plurality of microprocessors;

a shared resource; and

a controller coupled to the plurality of microprocessors and the shared resource by a first bus and a second bus, respectively, the controller including a register having a lock portion associated with each of the plurality of processors and a status portion, each of the lock portions indicating whether the associated one of the plurality of microprocessors has obtained access to communicate with the shared resource, and the status portion includes a bit indicating whether any of the plurality of microprocessors has obtained access to communicate with the shared resource; and

wherein each of the lock portions comprises an arbiter device which accepts lock bits input from each of the plurality of processors and outputs the lock bit of a processor that addresses the arbiter device.

2. (Original) The system of claim 1 wherein the shared resource comprises a memory device.

3. (Original) The system of claim 1 including a plurality of shared resources.

4. (Original) The system of claim 3 wherein the register includes at least as many lock portions and status portions as there are shared resources, wherein each shared resource has a lock portion and a status portion associated therewith.

5. (Canceled)

6. (Currently Amended) The system of claim [[5]] 1 wherein, when a particular processor requires access to the shared resource, it inputs a lock bit to the arbiter device.

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7. (Original) The system of claim 6 wherein, if no processor other than the particular processor has input a lock bit to the arbiter device, the arbiter device accepts the lock bit from the particular processor and enables the particular processor to access the shared resource.

8. (Original) The system of claim 7 wherein, when access to the shared resources is enabled, a status bit in the status slice associated with the shared resource is set.

9. (Original) The system of claim 6 wherein, if a processor other than the particular processor has previously input a lock bit to the arbiter device, the arbiter device clears the lock bit from the particular processor to zero.

10. (Original) The system of claim 9 wherein, when access to the shared resources is enabled, a status bit in the status portion associated with the shared resource is set.

11. (Original) The system of claim 8 wherein, after the particular processor inputs its lock bit to the arbiter device, the particular processor addresses the arbiter device to read its lock bit from the output of the arbiter device and reads the status bit associated with the shared resource.

12. (Original) The system of claim 10 wherein, after the particular processor inputs its lock bit to the arbiter device, the particular processor addresses the arbiter device to read its lock bit from the output of the arbiter device and reads the status bit associated with the shared resource.

13-31. (Canceled)